COMPONENT BASED APPROACH FOR INTEGRATED CIRCUITS

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Abstract: In this paper we propose the different physical-topologic fragmentation approach for VLSI, based on the object and software component technologies, which considerably shortens the computation capacity, consequently providing an increase in quality and circuit parameters improvement.

Key words: UML, software components, models, integrated circuits, granularity.

1. COMPONENT BASED CONCEPT FOR INTEGRATED CIRCUITS

The modern microelectronic device designing realized in unified cycle is very sophisticated thing, but this problem becomes more complicated because of physical limits, where seeking compromise between VLSI and VHSI, otherwise geometrical, thermodynamic and electrical limits is not independent but is correlated [1–3].

Most of the tools used in modern practice for analysis and design, are based on CAD

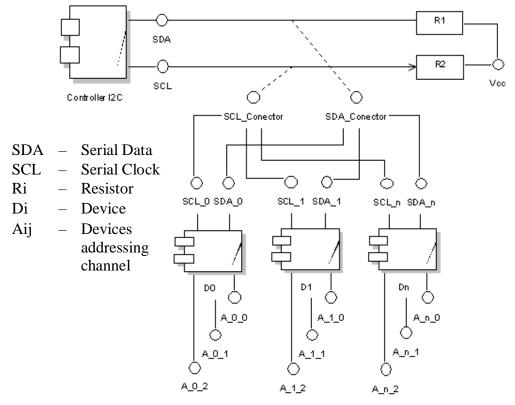


Fig. 1 – The connection of devices to the I^2C controller

(Computer-Aided Design) technologies, VLSI design being reduced either to functional-structural decomposition, or to the basic logic level. Similar approaches are not efficient, because of multiple complications of the model combinations on different analysis levels, taking into consideration the big amount of information in different processing fields (technological, topological, electrical, etc). The new approach that allows the perception and analysis on the macro level of the circuits is the component-based approach by using UML (Unified Modeling Language) [4, 5]. In this case, the components will be in consideration with the macro-granularity blocks, and they can mean either a large-scale circuit, or the whole device. The main objective and the critical difference of this approach, consists in system analysis based on software object and component technology (on different abstraction and detailed levels) for circuits as an integration matter (compatibility criteria). Software components concept allows us to distinguish the essential aspects and drop the unimportant ones, depending on the analysis level of the circuit. The analysis principles have a similar formulation as the Top–Down ones – on the superior levels the component granularity is small, respectively the number of dependencies (or links) between components is insignificant (Figure 1), but closer to the inferior levels granularity goes up – underlining more dependencies. The inferior level is the one where the logical elements are described in detail. But since these logic elements are distributed among components, the analysis becomes more clear and intelligent, because it is possible to make a generalized examination on the superior levels and a functional delegation on the inferior levels. The component based analysis and design is performed in UML, because the semantics and extension ability allows a successful use of mechanisms. The particular mechanism that allows the execution of models (in the definition of decomposition specific for integrated circuits (IC)) is of the stereotypes, which allow the determination of elements from which there will be composed the components on different levels. One of the advantages of using UML in such cases is the possibility to create intelligent systems for IC simulation, with the outlook for integration into a unified development and manufacturing system.

2. ANALYSIS AND REPRESENTATION OF INTEGRATED CIRCUITS INTO COMPONENTS

Component based analysis method of IC provides the decomposition of IC in subcircuits, for the purpose of inter–circuit dependencies examination. In this case the advantage offers the opportunity of circuits analysis, independently of transistors level. Therefore, the subcircuits are replaced with components, which are analyzed as black boxes. The analysis process represents a sequence of phases, where at each phase is made a transition to the next level of granularity (for element distinction on different levels there can be introduced stereotypes). On the first level, takes place the replacement of unilateral circuits with their one–way versions (Figure 2), performed in

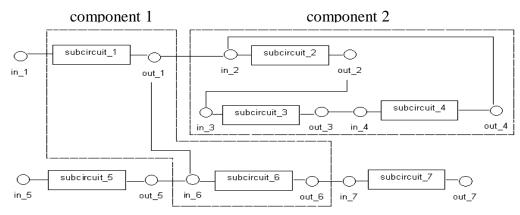


Fig. 2 - Replacement of unilateral circuits with their one-way versions

order to obtain a primary model with high granularity – the existence of feed–backs in this model is allowed (feed–backs can be initial reduced by removing the elements that provide similar dependencies). As a matter of fact, this model represents the transition phase from physical–dependent model of the circuit, where can be distinguish transistors, to the independent model.

On the next phase the component granularity was reduced (Figure 3) – this model has to be already without feed–backs. One solution for "hiding" the feed–backs can be the embedding of components that contain similar dependencies. Therefore, we obtain strongly–connected

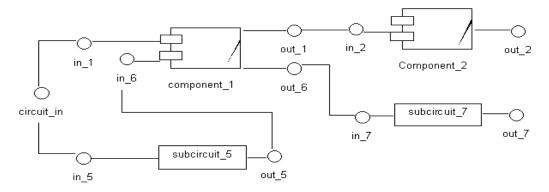


Fig. 3 – Reducing of feed-backs

components, where the feed-backs are kept, but on the current level they stay unstressed. Next phase may be optional: if unidirectional dependencies (arcs) exist on the preceding phase, then (on the current model) each unidirectional dependence needs to be substituted with a pair of directed dependences.

The obtained model is similar to the oriented graph, where input and output circuits are pointed out. The input circuit represents only one node, which is obtained from joining up all inputs, and the output circuit can be represented by more nods, where each output corresponds to only one node. When all transformations are done, the volume of model description will be reduced, thus simplifying the analysis method without decreasing the consistency of the IC model. In addition to this, the component models can be complemented and modified by an iteration process without computing the rest of the IC, and that aspect can remain unaltered as a result of various causes of design. Simultaneously, each component can be developed based on detailed models of IC elements (equivalent models, physical models of nano-levels or sub-microns, macro models, etc.) which can improve the designing process as a result of the in-depth study (and fundamental understanding) of physical processes, thus we can reduce computational power and resources.

Therefore, we obtain a more powerful physical-topologic fragmentation of IC, which reduces not only the developing phases but also the content of description, which by itself reduces substantially the volume of computations, ensuring the quality and an improvement of circuits parameters based on intelligent evaluation of simulation tests. The obtained results give us hope in the development of intelligent CAD systems.

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