CHARACTERIZATION OF SILICON P-I-N PHOTODIODE ELECTROPHYSICAL PARAMETERS

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Electrophysical parameters of test structures formed in high - resistivity silicon during manufacturing of p-i-n photodiodes have been investigated. Using specially designed metal-insulator-semiconductor (MIS) structures important electrophysical characteristics of $Si-SiO_2$ and $Si-SiO_2-Si_3N_4$ systems were examined. Surface generation velocity S_g, bulk generation life-time of minority carriers τ_g and fixed charge in the insulator Q_{ss} have been determined. These parameters reflect the quality of insulator-semiconductor interface and near surface semiconductor layer. The effect of insulator type on S_g values have been found. The influence of electric field in the insulator on generation of minority carriers in MIS structures was shown.

Designed test structures have proved their high effectiveness for investigation of generation parameters in p-i-n photodiodes.

Key words: p-i-n photodiodes, high-resistivity silicon, MIS structures, electrophysical parameters of silicon.

1. INTRODUCTION

The dark current in p-n junctions is an important characteristic of p-i-n photodiodes employed for detection of low signals. The main contribution to the dark current is caused by the volume generation of minority carriers in the depleted region of the p-n junction and surface generation at its periphery. Hence investigation of generation currents and their components is an important task in revealing the effect of construction and process parameters on performance of p-i-n photodiodes

2. EXPERIMENTAL.

MIS gated diodes and MIS capacitors formed during p-i-n photodiodes manufacturing have been used. Two groups of samples have been investigated with single and double layer insulator under the gate. The thickness of SiO_2 in case of single layer dielectric was about 4500Å. In case of double dielectric layer the thickness of SiO_2 and Si_3N_4 was 2000 Å and 600 Å consequently.

The area of square aluminium electrodes was equal $4 \cdot 10^{-2}$ cm^2. The rear side of the substrate was doped by phosphorus and aluminium film was deposited for creation of ohmic contacts. Effective concentration of doping impurity in high-resistivity silicon was in the range $(3\text{-}5) \cdot 10^{12}$ cm^{-3}. Two different constructions of MIS gated diodes have been used. In the first case the p-n junction, which served as a drain for minority carriers in non-equilibrium conditions, had small area (20x70μm) and partially was covered by the gate electrode. In the second case the p-n junction consisted of 20 long (about 2000μm) and narrow (10 μm) parallel stripes completly situated under the gate electrode. The first construction was used for τ_g determination while the second one was used for correct S_g analysis. In MIS gated diodes with branched p-n junction practically all minority carriers generated at the surface are collected by the drain and surface generation velocity is determined accurately.

S_g values have been calculated from the dependence of minority carrier generation current under the gate electrode on the inversion voltage [1,2]. Time dependent high-frequency capacitance relaxation curves (C-t) of MIS structures were used for τ_g investigations by Zerbst method [3]. Effective value of fixed charge in insulator was determined from high frequency capacitance - voltage characteristics.

3. RESULTS AND DISCUSSION.

Typical generation currents with distinct surface component in MIS gated diodes with branched p-n junction are shown in Fig.1. The shift in position of the surface generation peaks is caused by different threshold voltages in test structures with various types of gate insulator. Averaged S_g value in MIS structures with SiO_2 as a gate dielectric was 1.4 cm/s. In the case of double layer gate insulator (SiO_2-Si_3N_4) S_g was equal to 3.7 cm/s.. Possible explanation of the difference in the surface generation velocity may be connected with variations of process factors and thermomechanical stresses at the insulator-semiconductor interface. On the whole such S_g values reflect low concentration of surface states responsible for generation of minority carriers in MIS structures. Thus, surface generation component in the dark current of p-i-n photodiodes is also low. At the same time surface generation velocity measured in the MIS gated diodes with a small area of the drain p-n junction was essentially lower because of non effective collection of generated minority carriers.

Calculated τ_g values were in the range $(1.9\text{-}6.0) \cdot 10^{-3}$ s. Higher generation life-time is inherent to the MIS structures with SiO_2 as gate insulator. Estimated width of the silicon layer, within which τ_g has been measured, was about 50μm.

Detailed analysis of C-t characteristics and Zerbst plots has shown that in some cases the generation current dependence on the width of the space charge region in silicon is not monotonous.

Initial part of this process is characterized by low bulk generation velocity. At the final stage the relaxation process accelerates significantly. Such behaviour is connected with increased electric field in the dielectric and may reflect the presence of specific centers at the Si-SiO_2 interface responsible for increased generation rate of minority carriers.

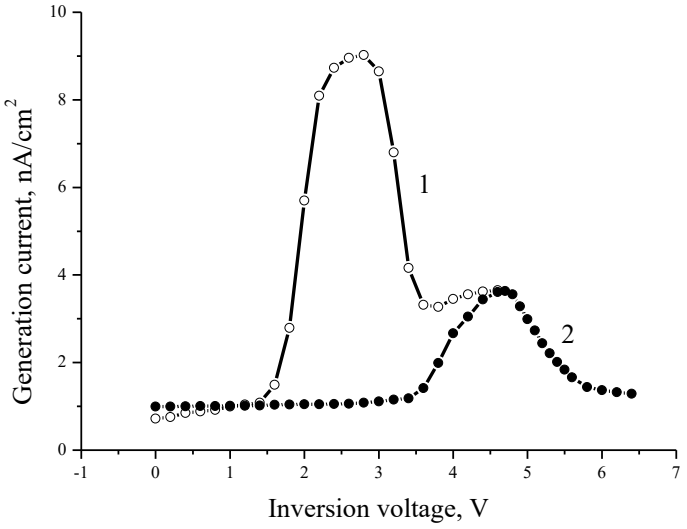

Fig.1. Generation currents in MIS gated diodes with double (1) and single layer (2) insulator. Drain voltage = – 2V.

Fixed oxide charge was found in the limits of ($2.5\cdot 10^{10}$ – $1.4\cdot 10^{11}$) cm^{-2}. Q_{ss} behaviour depended on the type of insulator and technological parameters of its formation.

4. CONCLUSIONS

Electrophysical characteristics of MIS structures formed on high resistivity silicon substrates during manufacturing of p-i-n photodiodes have been investigated. Generation parameters of the silicon near surface region and Si-SiO_2 interface were determined. Bulk generation life-time of minority carriers was found in the range $(1.9\text{-}6.0)\cdot 10^{-3}$ s and was an evidence of sufficient quality of silicon substrates. Surface generation velocity varied in the interval (1.4 – 3.7) cm/s and was significantly lower for MIS gated diodes with single layer insulator (SiO_2) than with double one (SiO_2-Si_3N_4). Fixed charge in dielectric was within the limits of ($2.5\cdot 10^{10}$ – $1.4\cdot 10^{11}$) cm^{-2}. Effectiveness of described test MIS structures for analysis of generation parameters of insulator-semiconductor systems in manufacturing of p-i-n photodiodes was shown.

5. REFERENCES

[1]. Fitzgerald D.J., Grove A.S.; (1968) Surf. Science; v. 9; №2; 347-352.
[2]. Grove A.S., Fitzgerald D.J.; (1966) Solid.-State. Electr.; v.9; №8; 783-789.
[3]. Zerbst M.; (1966) Z. Angew. Phys.; v.22; №1; 3039-3042.