Design and Partitioning Across 2 Strata in 3D IC architectures

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Abstract. The 2D tools used for producing integrated circuits can be adapted for de 3D integration taking into consideration the design, technological files and methodology used for implementation [1,2]. A suitable design for 3D integration using 2D instruments should have about half memory area and half standard cells area, memories going to the 2nd stratum and standard cells remaining on the 1st stratum [3]. Usually these 2 strata will have different placement utilization, but anyhow much smaller than 100% (this is very depended by design size and shape as well as by memories' size, shape and number). There are custom memories witch allow abutment ("touching each other") on 3 sides and such memories will allow abutment on all 4 sides in 3D placement and, in some cases, this can drive to 100% utilization on 2nd stratum. A different category of memories are the small ones which can remain on the 1st stratum along with standard cells [4]. The last to categories of memories are exception and depending on the blocks of memory used in the design there can appear more particular scenarios that need to be treated in a specific way [5].

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