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Aspects of generating the tests in the DALG-I concept

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Abstract - Once with the enhancement of the integrated circuits (IC), the number of tests and the time of creating them was augmenting much, and the detecting errors tests from the ccombinational circuits (CC) with convergent fan-out (CFO) couldn't be created in the DALG-I concept of activating the unique path through the circuit [1]. To solve this deadlock there are proposed 2 ways: 1) the projection for testability (PFT) of CC; 2) the elaboration of efficient algorithms to create the tests, which allows a fast easy way to create tests for different structures and the diminuation of number of tests. Because PFT needs long term and complex studies, the second variant was choosed: it was proposed the algorithm DALG-II of creating the tests [2], based on the simultaneous activation of all the paths CFO. The article presents the results of a study of creating the tests based on the principle DALG-I and the causes of the presence of the effects of compensation or masking the errors mentioned in [1].

INTRODUCTION

The necessity of permanent amelioration of the functionality of IC leads to the augmentation of it's complexity, of it's degree of difficulty of creating the tests and of the time of creation, which can pass over 10-15 months. Furthermore, in accordance with [1] the creation of tests for some CC with FOC cannot be done with the method of activation of the unique path (MAUP) through the circuit. It has been in discussion the elaboration of some efficient algorithms for creation the tests, which can solutionate these problems. Roth [2] has elaborated the DALG-II algorithm for creating the tests, which allows the creation of tests, which allows the creation of the test in all the cases, when it exists [3]. The starting point for the DALG-II was the concept of simultaneous activation of all paths CFO through the logical gate (LG) of convergence (LGC), until all the observable outputs of CC, which eliminates the disastrous consequences of the DALG-I [3]. The efficiency of the DALG-II was demonstrated with only one test for the Schneider circuit. At the same time, from the aparition of the DALG-II there were doubts [3] regarding the rectitude of taking some conclusions regarding the efficicency in creating one test of detecting an error, maybe specific, for CC from [1]. In [4], it was demonstrated that the Schneider CC is a special CC: the logical gate 6, also it's output (whose analyzed error 6≡0 is a specific one) are redundante. Also, is not clear why the efficiency of DALG-II wasn't demonstrated also for the oposite error 6≡1. More than this, DALG-I and DALG-II are reffering to diferent types of situations, which till now weren't or were less analyzed in the specific literature: 1) DALG-I is based on MAUP and on the model of singulier constant error (SCE), these leading to create a new set of diagnosis tests; 2) DALG-II is based on the simultaneous activation of all paths from the point of fan-out FO through the (LGC) to all the observable outputs of the CC, and by default, on the model of multiple constant error (MCE), which leads to the creation of verification tests. Or the interaction of MCE of CC with FOC with similar or oposite parities of the signals with the properties of the logical gate (LG) of convergence are potential sources of apparition of the compensation or masking effect of the errors.

I. BASIC CONCEPTS AND BASIC DEFINITIONS

The testing of a CC means making an experiment in which the inputs of the CC are applied to the sequence of stimulus vectors of the binary signals of input, chosed in a certain way, and at the outputs there are observed the respectives reactions. The efficiency of a testing process depends on the properties of the logical signals, on the logical properties of the LG, of the functional and structural properties of the CC and on their interaction.

I.1. The properties of signals and of logical ports

Betwen the logical values of the input signals of a LG with n inputs and the output signal there are some relations. For example, the logical value (LV) 0 (1) applied to only one input i, $i = (\overline{1,n})$ of LG AND (OR) determines uniquely the logical values LV 0 (1) at the output of the gate.

Definition 1. The LV of the input signal which, no matter of the values of the others signals of the LG inputs, determines uniquely the signal at the output of the LG and is called dominant LV (DLV) (of blocking). We will assign VLD on the connexion **i** trough ***i=d***.

Definition 2. The uniquely LV of the output signal of a LG, which is different from all the others LV of the output signal of this LG, it is called equivalent LV (ELV) (homogene). LG AND (OR) have the equivalent LV (ELV) of the output signal 1 (0). We will assign ELV at the output ***s*** of the gate through ***s=e***.

Definition 3. It is called an equivalent set (homogene) of the values of the binary signals the stimulus vector (SV) ee..e of the values of the input signals, which

corrresponds to the unique ELV of the output signal of the **s** LG. We will assign ELV on the connexion **i** through ***i=e***, $i = \overline{(1, n)}$, (1)

Definition 4. The LV of each binary variable of the equivalent set (homogene) it is called ELV of the input signal of the gate. For example, if the gates with 3 inputs AND (OR) equivalent set of the values of the input signals will be the set 111 (000). It results that 1(0) will be ELV of the input signal of this gate. In the case of the LG with inverter at the output ELV to the input and the output LG will be oposite. The equivalent set (ES) has the following properties:

1) each component of the ES ***ee..e,*** $i \in \{1, n\}$ represents a potential LV of manifestation (M) of the errors of type *i≡d*; all other components of the set *ee..e*, without the one of the connexion ***i≡d,*** represents the condition of unique propagation (UP) of the signal, correct or eronated, of the connexion ***i*** trough this input till the output of the gate;

2) ES ***ee..e*** of the LG has the maximum capacity of detection: it can detect SCE of type *i≡d,* $i \in \{1, n\}$ of the signal of any input connexion of the LG. So, a single SV can detect the errors of type *i≡d* of any of the n inputs of the LG;

3) ES can detect the presence of an error of type *i≡d* at one of the inputs of the LG, but are not locating a certain defect input. This property of a LG and there are no modalities, except the one related to the structure modification (auxiliar control points or auxiliar logic), for passing trough from this situation.

Definiția 5. The errors detected by ES of the signals of the stimulus vector are called equivalent errors.

Definiția 6. SV of the values of the input signals of the LG, which contains a dominant signal at one input, and in the others inputs of the equivalent signals is called dominant set (DS). The repective reaction when on apply DS will be *d* ($\bar{d}$). For example, for the gates with 3 inputs AND (OR) the dominant sets of the values of input signals will be: *d11*, *1d1* and *11d (d00, 0d0, 00d)*. It result that LV of the signal M of the error will be *d*, and the verified error will have the oposite value, which is *e*.

DS has the following properties:

1) each DS is senzitive to the binary signal of one single input *i*, that means the one that contains the dominant signal *i=d*. The changing of this in the oposite at the *i* input assures the condition of M of the error *d→e*, adică *i≡e*. The signals of type *e* at all the other inputs of the LG assures the condition of UP of the signal, correct of eronated of the input i, till the output of the gate;

2) DS *de..e* has the minimum capacity of detection: it can detect one single error of type *i≡e,* $i = \overline{(1, n)}$. So, for a gate with n inputs will be necessary n stimulus dominant vectors (SDV) for detecting the errors of type *i≡e* at all the inputs of the respectives LG;

3) Each SDV and the respective reaction at the output of LG contains a detection test and also one of locating of error of type *i≡e*.

From the property 2) of the equivalent set and the property 2) of the dominant set it results the theoreme 1.

Teorema1. The ensemble T_d of detection test of the error of one logical gate AND (OR) contains (n+1) tests, where n is the number of inputs.

Demonstration:

We suppose that $T_d \neq (n+1)$ tests. That means:

1) T_d does not contain any equivalent test (T_e=0) or it contains more than one equivalent test T_e>1. That means, is not like the definition of ES. From here it results that it is only one ES of detecting all the equivalent errors (*i≡d*) of the inputs of LG;

2) T_d contains a number of dominant tests $T_{dom} \neq n$. That is not like the property 2) of the DS: for a gate with n inputs it exists exactly n dominant tests, each of these showing the error of type *i≡e* at the respective input.

From 1) and 2) it results that:

$$T_d = T_e + T_{dom} = (n+1) \text{ teste} \quad , \qquad (2)$$

From the Theoreme 1, the properties of the logical gates and the properties of the equivalent and dominant sets follows:

Corollary 1.

The set of tests $T_d = (n+1)$ represents a small unique ensemble, minimal and complete of detecting and diagnosis tests of errors of one gate with n inputs.

Corollary 2.

The apparition of each SCE *i≡d,* $i \in \{1, n\}$ leads to the modification of set T_e in the set T_{dom} and respectively the change in oposite of the value of the signal at the output of the LG.

In similar way, the apparition of any SCE *i≡e,* $i \in \{1, n\}$ leads to the modification of set T_{dom} in set T_e and the changing in oposite of the value of signal at the output of the LG.

Corrolary 3. The effect caused by the simultaneous propagation of signals of 2 or many paths of the FOC with oposite parities, which leads to the replacement of one set T_{dom} = ***ed*** of detection of error k***0*** with other set T_{dom} = ***de*** of error k***≡1*** it is called ***compensation of error***. So, also in the absence of the error, as in it's presence the reaction at the output of LG will be the same, the test for the respective error being impossible for creating. This was caused by the insuficiencies of the DALG-I and leaded to the fundamentation of necessity for establishing an efficient algorithm [1,2]. The veridicity of this afirmation is debatable. In fact, the effect of compensation suppose the simultaneous propagation of error by different paths with oposite parities of signals, which by default leads to the model of MCE, whilst the DALG-I is based on the SCE.

Masking of error appears in the case of circuits with logical redundance and is caused by the eronated presence of a signal ***d*** at one input of the LG, which leads to the impossibility to obtain the homogene set.

I.2. The functional and structural properties of the CC

A logical function (LF), in dependence with the analytical way of representing it – without repetion of some input variables, with their repetition or with the repetition of input and intern variables – can be represented with the following types of CC:

1) irepetitive CC (without FO).

2) repetitive structures (only with FO of the primary inputs).

3) aribitrary structures (general) – with FO of primary input and internal connexions.

The functionality of a CC is determined from the specifical interaction between the LG and the way of organising the inputs and outputs of CC.

It exists a bivalent corespondance between the analytical representation of one LF and the numerical structure, who realise this LF. The graphical representation of CC is, in the general case, more comprehensive and allows the easy detection of specifical properties of some certain type of structure. The totality of a SV of input signals and of respective reaction at the CC output is called ***test***. The creation of a error detection test needs the accomplishement of 2 conditions:

1) the manifestation (M) of error of connexion supposed defect, which means the installation on this connexion of the oposed logical of the supossed error;

2) UP of the corect or erronated signal till one observable output, which means the appliance of the ELV of signals at all the inputs of LG, trough which passes the activated path. The functional and structural properties of one CC must be studied from point of view of the primordial of granting the conditions M and UP of the correct or erronated signal on the connexion supposed defect till the observable outputs of the CC. In the general case, the impossibility of granting the condition M of error means the impossibility of controlability calculus (C) of the respective connexion, which means the inexistance of some combination of logical input signals, which can allow the installation of desired logical value of the signal on the considered connexion. By default, this leads to the impossibility of establishing the verification test of the respective error of the given connexion. The impossibility of granting the UP condition of the correct or erronated signal from the connexion supposed defect till the observable outputs of the CC means the impossibility of estimating the observability (O) of the respective connexion, exactly the inexistance of some combination of the input signals, which would allow the installation of ELV at all the inputs of the LG trough wich it passes the inverse activation path from the ouptut connexion of the CC to the connexion whose O would like to be observed. By default, in this situation also leads to the impossibility of establishing the verification test of the respective error of the considered connexion.

The number of inversations, applied to one logical signal at its propagation trough the LG of a CC, caracterises the parity of the logical signal at the output connexion in rapport with its parity on the initial connexion. The parity of a logical signal can be even or odd depending on the number even or odd of inverters trough which it was propagated. For the comodity of caracterising the parity of logical signals of some paths we will utilize the terms similar even and oposite even.

II. THE TRAPS OF AD-HOC DESIGN

For proving some aspects of testing, some authors utilize logical structures obtained in the intuitive way and not based on the sinthese methods well formalized. For example, in [5] (pag. 25, fig. 2.9,a), the proving of the efficiency of the D algorithm is made based on the CC from the figure 1.a. With a close look, it can be observed that this CC is equivalent to the circuits from the fig. 1.b and fig 1.c. From fig 1.c it results that the gates G_6 şi G_7 and the aferent outputs (see fig 1.c under the interrupted line) are *redundant*.

Same result can be obtained also in analytical form:

$$f = \overline{\overline{a \cdot b \cdot c} \vee \overline{b \cdot c \cdot c}} = (a \cdot b \cdot c) \cdot (b \cdot c \cdot c) = a \cdot b \cdot c \quad , (3)$$

From (3) it is clear that the circuit from fig 1.a wasn'tsynthetized conform to the formalized methodes of

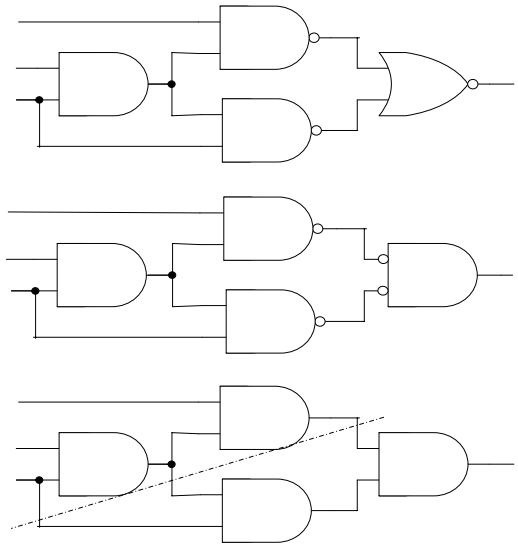

Fig. 1. The scheme utilized in [5] (pag 25, fig 2.9a) for proving the efficiency of the D algorithm)

canonical synthese: instead of one gate AND with 3 inputs it was utilized a redundant circuit with 4 gates, a FO of the primary inputs and a FO of the internal connexion. Normally the proving of some aspects of testing will be efectuated just from the logical structures obtained from the methods well formalized of minimalization and synthese of the LF. Otherwise, it will appear the risk of logical redundance (LR) and of function incompatibilities. LR is not the only danger of the ad-hoc structures: often the functionality of some CC obtained ad-hoc cannot be realized when using the formalized methods of minimalization and synthese. The sequel of this functionality can be desastrous. That's why the conclusions and the recomandations regarding different aspects of testing will be effectuated just for the CC obtained in conformation with the actual methods of minimalization and synthese.

III. ASPECTS OF CREATING THE TESTS FOR CC WITH CONVERGENT FAN-OUTS

The problem of interaction of FOC errors with the values of the dominant and/or homogene signals of LG in the case of SCE and MAUP will be solutionated exclusively in conformity with the exigences of the well formalized methods of minimalization and synthese of CC.

3.1. The interaction of convergent fan-out errors of CC in the DALG-I

In the case of the SCE and DALG-I will be activated a path to the observable output of the CC, which will lead

to the obtaining of a set of diagnosis tests. In this case it does not appear the interraction of constant errors, the tests of diagnosis being obtained easily, although thier number augments significantly once with the number of gates of the CC. Simultaneously, in the case of utilisation of DALG-I method there will be allocated priority to te granting of base principles – granting M to errors of the connexion supposed defect and the granting of UP of the signal of tested connexion till to an observable output.

This means that in the case of propagation of signal of connexion supposed defect to one of the paths, the signals of other paths of the FO must have at the entrance of the convergence gate LV the values ***e***, and not the value ***d***, which could block the unique propagation of the signal tested PLG.

3.2. The study of a CC with fan-out with oposite parity of signals and convergence gate of type OR

Being given FL f_1 from the Karnaugh table (fig 2.a). In conformity with the formalized methodes of minimalization and synthese it was obtained a CC with FO with oposite parity of signals and convergence gate of type OR. (fig 2.b). In the case of the SCE model and

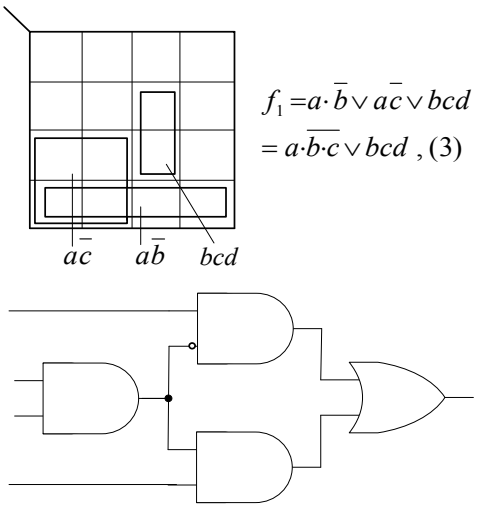

Fig.2. CC with fan-out with oposite parities of convergence signals and LG of AND type

was efectuated the creation of tests of detection/locating errors of connexion 5 with FO with the oposite parities and analyses the possibility of these 2 types of errors *5≡0* şi *5≡1* there were created 2 tests: one for each path of propagation of the signal of fan-out. When creating each

$T_1^c =$

$T_1^e =$

$T_2^c =$

$T_2^e =$

test there were assured the condition of error manifestation, resulting from the type of error, that the unique propagation condition of signal of connexion supposed defect. After the phase of forward tracing, in the purpose of definitivating the logical values of the signals remained unfinished, it was made the phase of backward tracing. In the process of synthesis of tests there weren't irresolvable logical conflicts or effects of compensating the error. Because LR of CC was excluded from the start, the masking of errors is not possible.

3.3. The study of a CC with fan-out with oposite parity of signals and convergence gate of type AND

Being given FL f_2 from the Karnaugh table (fig.3,a). In conformity with the formalized methodes of minimalization and synthese it was obtained a CC with FO with oposite parity of signals and convergence gate of type AND. (fig 3.b). In the case of SCE model and DALG-I principle it was made the creation of tests of detection/locating the errors of connexion 5 with FO with oposite parity and analysed the possibility of apparition of error compensation effect, forwarded in [1].. For each of the 2 types of errors *5≡0* şi *5≡1* there were generated

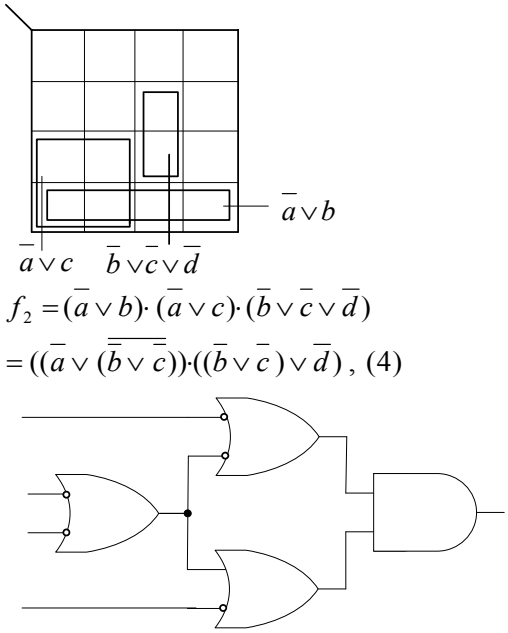

Fig. 3. CC with fan-out of oposite parities of signals of convergence and LG of AND type

2 tests: one for each path of propagation of the signal

$T_1^c = 1\,1\,1\,1\,1\,1\,1\,0\,1\,1$ In absence of error $5 \equiv 0$

$T_1^e = 1\,1\,1\,1\,0\,0\,0\,1\,0\,1$ In presence of error $5 \equiv 0$

$T_2^c = 1\,0\,1\,1\,0\,0\,0\,1\,0\,1$ In absence of error $5 \equiv 1$

$T_2^e = 1\,0\,1\,1\,1\,1\,1\,0\,1\,1$ In presence of error $5 \equiv 1$

from FO. In the process of synthesis of tests there weren't irresolvable logical of effects of compensating the error. Because LR of CC was excluded from the start, the masking of errors is not possible.

REFERENCES

[1] Roth J. P. Diagnosis of Automata Failures: A calculus and A Method. - IBM Journal of Research and Development, vol. 10, p. 278-291, 1966.

[2] Schneider P. R. Counterexample On the Necessity to Examine D-Chains in Diagnostic Test Generation – An exemple, IBM Journal of Research and Development, vol. 11, No.1, p. 114-115, 1967.

[3] Roth J. P., Bouricius W. G., Schneider P. R. Programmed Algorithms to Compute Tests to Detect and Distinguish Between Failures in Logic Circuits. - IEEE Trans. On Electronic Computers, vol. EC-16, No. 5, p. 567-579, 1967.

[4] Chang H. Y., Manning E., Metze G. – Fault diagnosis of digital systems. – Wiley-Interscience, New York, London, Sydney, Toronto, 1970.

[5] P. K. Lala. An Introduction to Logic Circuit Testing. Ebook. www.morganclaypool.com