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Towards Uniform Electrochemical Porosification of Bulk HVPE-Grown GaN

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In this paper, we report on results of a systematic study of porous morphologies obtained using anodization of HVPE-grown crystalline GaN wafers in HNO_3, HCl, and NaCl solutions. The anodization-induced nanostructuring is found to proceed in different ways on N- and Ga-faces of polar GaN substrates. Complex pyramidal structures are disclosed and shown to be composed of regions with the degree of porosity modulated along the pyramid surface. Depending on the electrolyte and applied anodization voltage, formation of arrays of pores or nanowires has been evidenced near the N-face of the wafer. By adjusting the anodization voltage, we demonstrate that both current-line oriented pores and crystallographic pores are generated. In contrast to this, porosification of the Ga-face proceeds from some imperfections on the surface and develops in depth up to 50 μm, producing porous matrices with pores oriented perpendicularly to the wafer surface, the thickness of the pore walls being controlled by the applied voltage. The observed peculiarities are explained by different values of the electrical conductivity of the material near the two wafer surfaces.
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Due to excellent properties, which include wide direct bandgap, high thermal stability, high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown field, low thermal impedance and superior chemical and physical stabilities, gallium nitride (GaN) has become a material of choice for a wide range of applications in optoelectronics and high-power/high-frequency devices, such as light emitting diodes (LEDs) for solid-state lighting[1] and visible light communications (VLC),[2] laterally diffused metal oxide semiconductor (LDMOS) radio-frequency devices for mobile communication[3,4] and radar applications.[5] Besides, high performance characteristics of GaN power devices make them promising for automotive applications.[6]

Nanostructuring of GaN, particularly by using electrochemical (EC) etching, enlarges the areas of applications toward surface enhanced Raman scattering platforms,[7–10] energy storage,[11] photocatalytic,[12,13] water splitting[14,15] and hydrogen generation applications,[16] photodetectors,[17–19] chemical and gas sensors,[20–24] photonic engineering,[25–30] waveguides[31] and Bragg reflectors,[32–35] and other novel intriguing applications. Note that EC etching is generally a unique approach to micro/nanomachining III-V semiconductor compounds for various purposes.[36,37]

For many concrete applications it is necessary to integrate a large amount of nanowires in one bundle or array to achieve required functionalities. Over the last decade, different template-based nanofabrication approaches have been developed which offer the possibility to produce large assembles of nanowires and nanotubes of various materials with defined diameters and lengths. Two types of templates are widely used for nanofabrication purposes, namely porous Al_2O_3[38–41] and etched ion track membranes based either on inorganic materials or on organic polymers.[42,43] Both, porous Al_2O_3 and etched ion track membranes, however, exhibit high resistivity and therefore they often play a passive role in nanofabrication processes. In particular, templated growth of nanowires via electroplating is provided usually by the metal contact deposited on the back side of the high-resistivity membranes, while electroplating of metal nanotubes requires additional technological steps e.g. chemical modification of the inner surface of the pores prior to electrodeposition which leads to the incorporation of spurious phases in the nanotube walls. In this connection an important technological task is the development of cost-effective semiconductor nanotemplates which properties could be easily controlled by external illumination, applied electric fields etc. We have developed a cost-effective technology for controlled fabrication of semiconductor nanotemplates with self-organized quasi-ordered distribution of nanochannels using anodic etching of some III-V (GaAs, InP) and II-VI (CdSe) crystalline substrates in a neutral electrolyte.[44–46] The high conductivity of the semiconductor nanotemplate skeleton provides conditions for uniform electrochemical deposition of metal species on the inner surface of pores, resulting in the formation of arrays of metal nanotubes embedded in semiconductor matrix.[44]

The electronic band gaps of InP, GaAs and CdSe are 1.3; 1.4 and 1.7 eV at 300 K respectively, which means that the nanotemplates based on these materials are opaque in the visible region of the spectrum. At the same time GaN with the bandgap as high as 3.4 eV at 300 K is feasible for the fabrication of conductive nanotemplates transparent in the whole visible region of the spectrum.

However, despite the expanding applications, the subject of GaN nanostructuring by EC etching still needs better understanding for a wider exploration of novel nanostructures and devices,[47] especially those requiring porosification in-depth of GaN wafers.

All the produced up to date porous GaN layers are limited to around 2 μm in depth. This is due to fact that, for a long time, GaN has been grown by Metalorganic Chemical Vapor Deposition (MOCVD) on sapphire, Si, or SiC for research and device applications. The thickness of such layers is usually limited to 2–3 μm, and the produced layers suffer from internal strains and defects due to significant mismatches of crystal lattices and thermal expansion coefficients with the substrate material.

Nowadays, there are three main technologies used for GaN bulk crystal growth: hydride vapor phase epitaxy (HVPE), sodium flux and ammonothermal growth.[48] Among these methods, HVPE growth appears to be the best choice, since the ammonothermal growth seems to be inappropriate for mass production of GaN crystals, providing

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